Electronic Version
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# Claims

[c1] A dynamic random access memory (DRAM) storage device, comprising:
a storage cell having a plurality of transistors arranged in a gain cell configuration, said gain cell coupled to a read bitline and a write bitline; and
a dummy cell, said dummy cell configured as a clamping device for said read bitline, wherein said dummy cell opposes a read bitline voltage swing during a read operation of said storage cell.

[c2] The storage device of claim 1, wherein said dummy cell further comprisesat least one transistor corresponding in the configuration thereof to said plurality of transistors of said storage cell.

[c3] The storage device of claim 1, wherein said storage cell and said dummy cell are further configured in a three-transistor (3T) arrangement.

[c4] The storage device of claim 1, wherein:
a gain transistor of said dummy cell is configured to supply current to said read bitline when the voltage on said bitline drops, from an initial precharge voltage, in

an amount at least equivalent to the threshold voltage of a write access transistor of said dummy cell.

[c5] The storage device of claim 1, wherein said dummy cell further comprises a write access transistor having a gate terminal coupled to a nominal logic supply voltage, $V_{DD}$, one of a source and drain terminal coupled to $V_{DD}$, and the other of said source and drain terminal coupled to said read bitline.

[c6] The storage device of claim 1, wherein:
said storage cell is coupled to a read wordline and a write wordline; and
said dummy cell is coupled to a dummy read wordline and a dummy write wordline.

[c7] The storage device of claim 6, wherein during a read operation of said storage cell, said dummy read wordline is activated at the same time as said read wordline.

[c8] The storage device of claim 1, wherein a write access transistor within said dummy cell has one of a source and a drain terminal coupled to a nominal logic supply voltage, $V_{DD}$, and a gate terminal coupled to a wordline-boosted voltage,$V_{PP}$, wherein $V_{PP}$ is higher that $V_{DD}$ by an amount at least equal to the voltage threshold of said write access transistor.

[c9] A method for clamping a read bitline of a gain access dynamic random access memory (DRAM) device having a plurality of storage cells associated therewith, the method comprising:
configuring a dummy cell as a clamping device for the read bitline, wherein said dummy cell opposes a read bitline voltage swing during a read operation of one of the plurality of storage cells.

[c10] The method of claim 9, wherein the storage cells and said dummy cell are further configured in a three-transistor (3T) arrangement.

[c11] The method of claim 9, further comprising:
configuring a gain transistor of said dummy cell to supply current to the read bitline when the voltage on the bitline drops, from an initial precharge voltage, in an amount at least equivalent to the threshold voltage of a write access transistor of said dummy cell.

[c12] The method of claim 10, wherein said dummy cell further comprises a write access transistor having a gate terminal coupled to a nominal logic supply voltage, $V_{DD}$, one of a source and drain terminal coupled to $V_{DD}$, and the other of said source and drain terminal coupled to the read bitline.

[c13] The method of claim 9, further comprising:
coupling the storage cells to a read wordline and a write wordline; and
coupling said dummy cell to a dummy read wordline and a dummy write wordline.

[c14] The method of claim 13, further comprising activating said dummy read wordline at the same time as said read wordline during a read operation of one of said storage cells.

[c15] The method of claim 9, wherein a write access transistor within said dummy cell has one of a source and a drain terminal coupled to a nominal logic supply voltage, $V_{DD}$, and a gate terminal coupled to a wordline-boosted voltage,$V_{PP}$, wherein $V_{PP}$ is higher that $V_{DD}$ by an amount at least equal to the voltage threshold of said write access transistor.

[c16] The method of claim 14, further comprising:
during a power-on phase, activating said dummy write wordline so as to store a voltage within a dummy storage node.

[c17] The method of claim 14, further comprising:
periodically activating said dummy write wordline so as to maintain a voltage within a dummy storage node.

[c18] The method of claim 17, wherein said periodically activating said dummy wordline coincides with a refresh operation for the plurality of storage cells.